

Circuit Architectures for Basis-Space Sampling in UWB Applications

Brian Dupaix and Steven Bibyk (PI)
dupaix.2@osu.edu bibyk.1@osu.edu

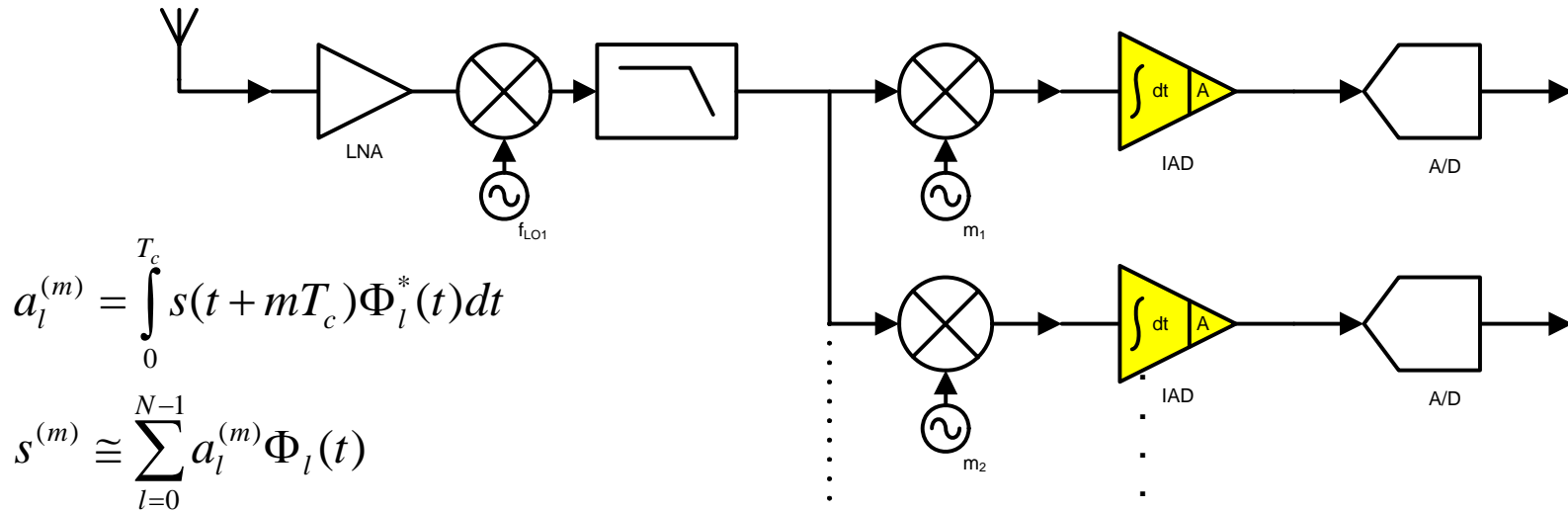
Continuing Project

Sponsor: Army Research Labs (ARL)

- **UWB Signals**
 - FCC: +500MHz bandwidth (minimum).
 - Capable of High Data Rates ($C=B*\log(1+S/N)$) in low S/N environments
 - Multipath Immunity
- **Nyquist delta function sampling difficult for UWB frequencies**
 - Nyquist = $2*\text{bandwidth} = +1\text{GSPS}$ – Prohibitive for single A/D systems
 - S/H aperture is a greater percentage of sampling period.
 - Analog sampling accuracy is more difficult as IC feature sizes decrease.
- **Goal: Reduce A/D Sampling requirement**
 - Evaluate A/D sampling methods effectiveness for 10GHz UWB system
 - Create architecture implementable in analog hardware

- **Align Sampling Theory with Analog Circuit evolution**
 - Targeting ultra-wide bandwidth systems.
 - Match to circuits in deep submicron processes
- **Match Basis-Space Sampling to Analog Circuits**
 - Use both signal projection and generalized sampling theory
 - Use integrated input samples rather than point (delta) function samples
 - Include basis function change of amplitude
 - Include developments in parallel sampling
 - Simplify analog baseband circuits
 - Signal integration attenuates jitter effects in parallel sampling

This architecture projects the received signal over a set of basis functions



$$a_l^{(m)} = \int_0^{T_c} s(t + mT_c) \Phi_l^*(t) dt$$

$$s^{(m)} \cong \sum_{l=0}^{N-1} a_l^{(m)} \Phi_l(t)$$

$(a_l^{(m)})$ - Basis Coefficient, $\Phi_l(t)$ - Basis Function, $s^{(m)}$ - Signal at time m

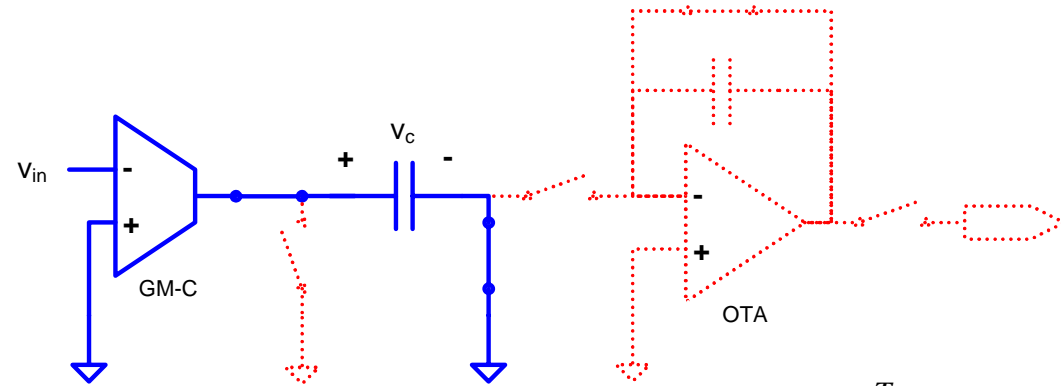
Basis Space Receiver

- Reduced A/D conversion rate
- Reduced Jitter Effects
 - Wide Aperture Sampling
 - Sample is integration period (T_c) wide
- Defined Filter – Integration
 - Well Adapted to Analog Hardware

Requires New Component

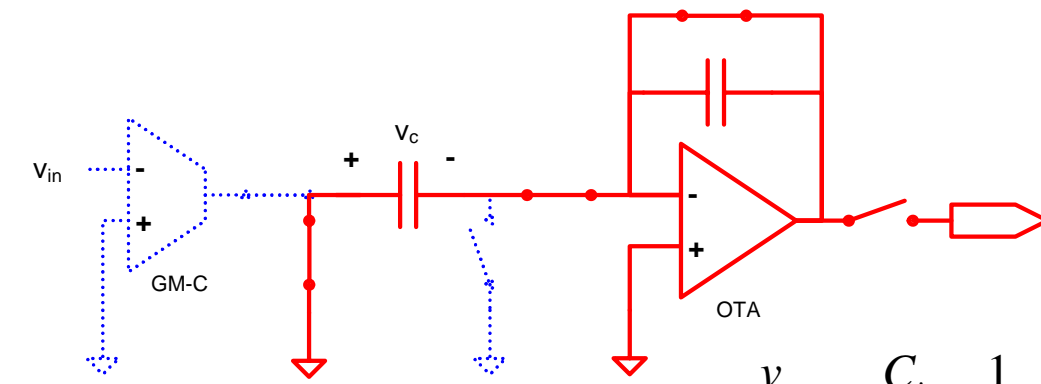
- Wide Bandwidth Integration (~100MHz)
- Provide Amplification
- Hold value for A/D conversion

Integrate-Amplify Dump (IAD)



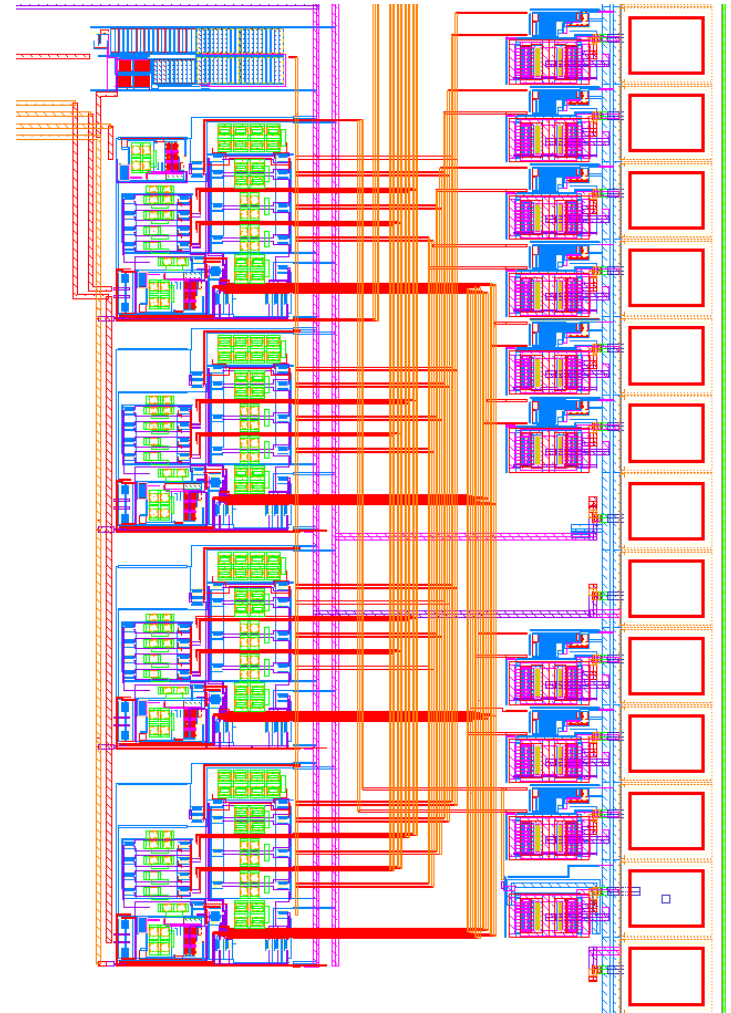
Continuous Time Integration

$$v_c = \frac{1}{C} \int_0^{T_c} g_m v_{in} dt$$

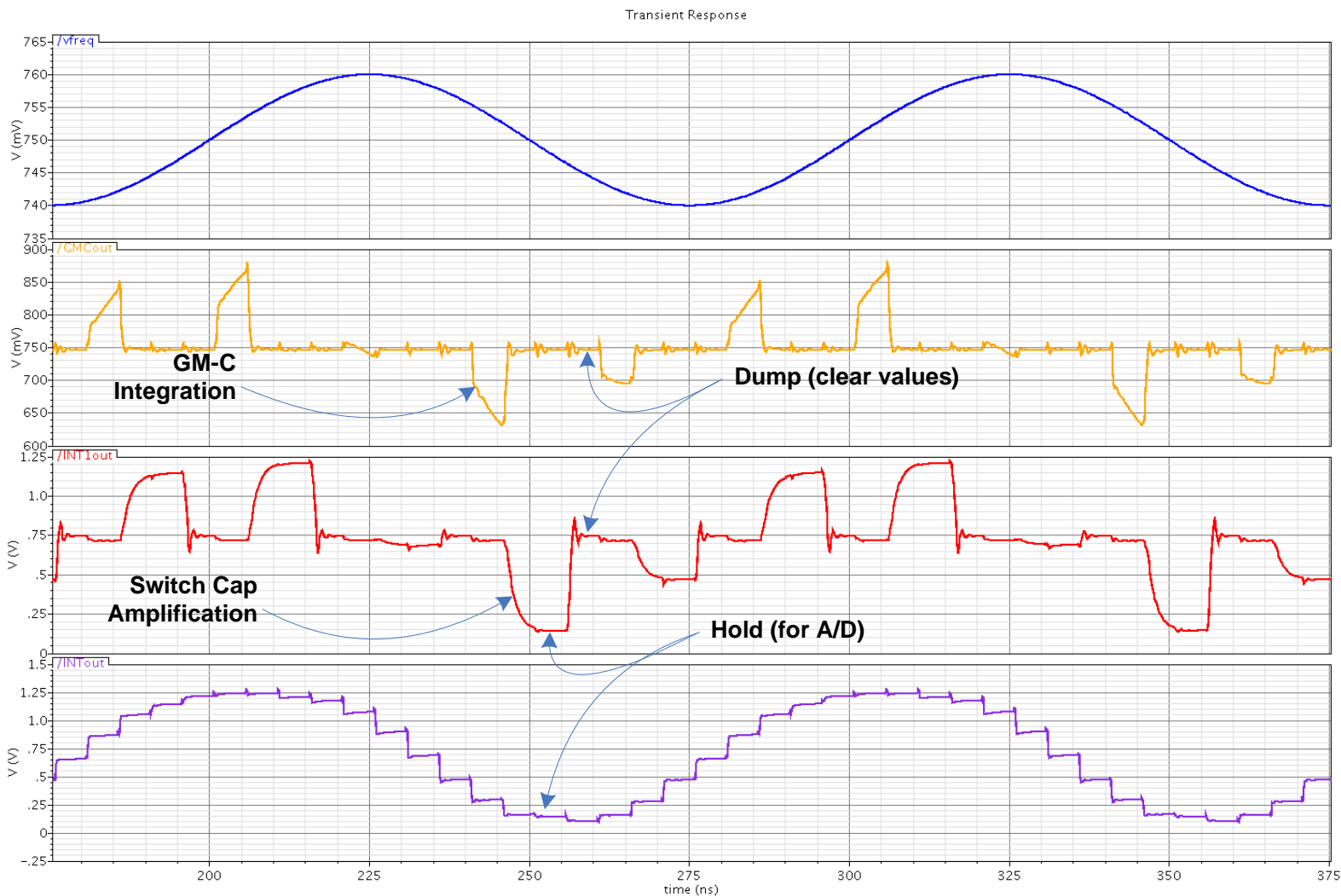


Switched-Cap Amplification

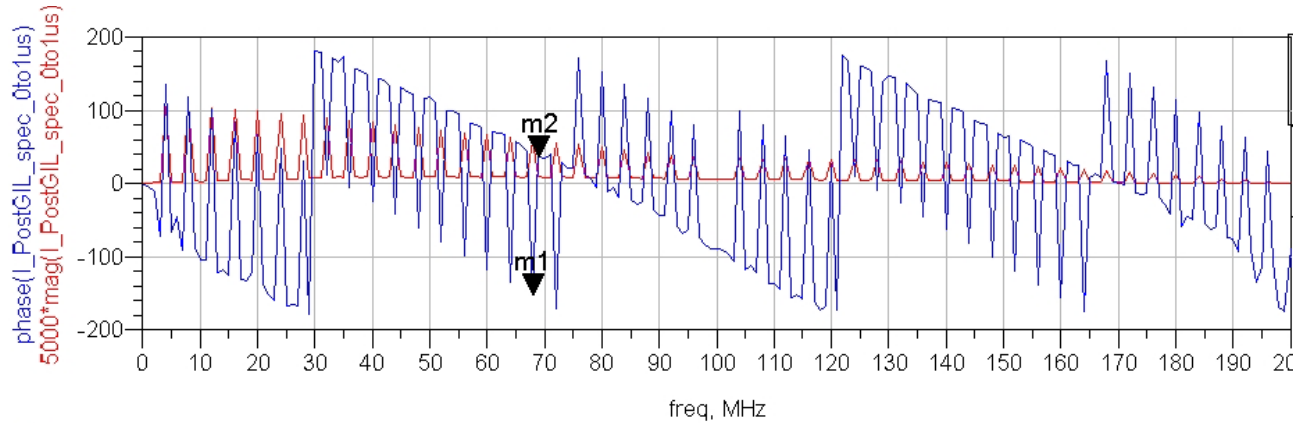
$$\frac{v_{out}}{v_{in}} = \frac{C_{in}}{C_f} \frac{1}{z-1}$$



IAD Layout in IBM 0.13um RF process

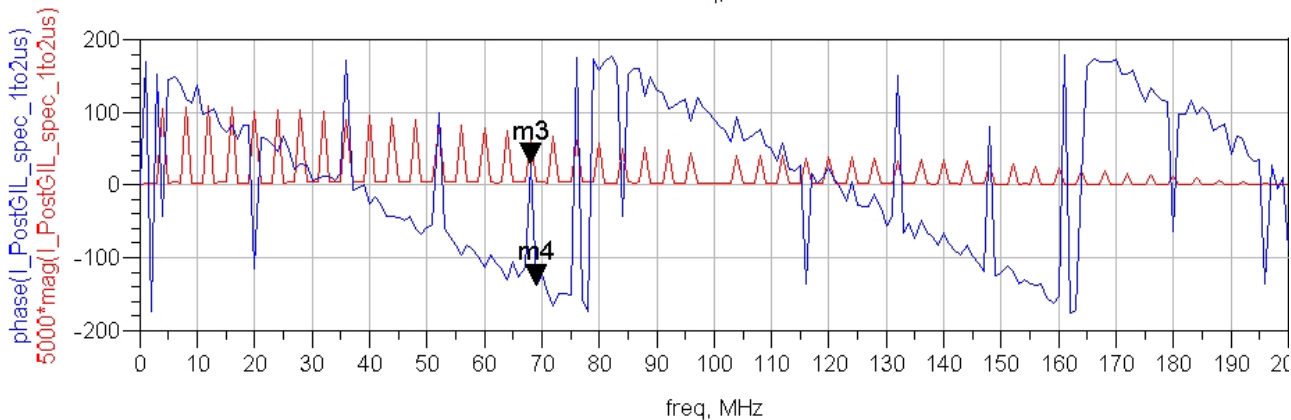


20MHz input; Integrate, Amplify, Hold, and Dump Timeperiods – 5ns



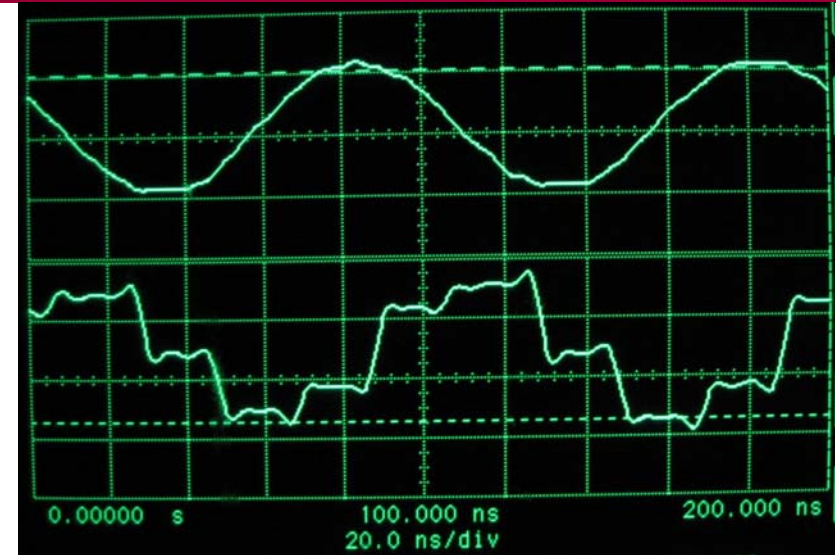
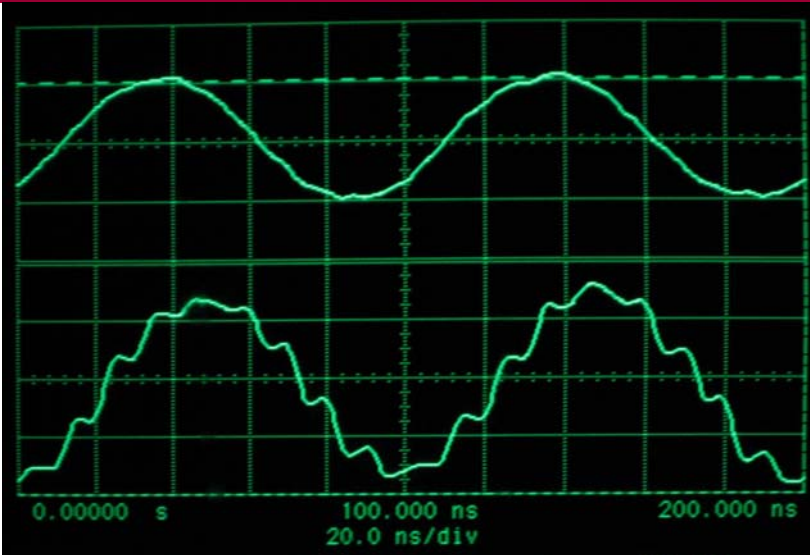
IAD Output with 24-4MHz Tones (OFDM signal) input.

Magnitude and Phase preserved.



IAD Output with 24-4MHz BPSK Tones (OFDM signal) input.

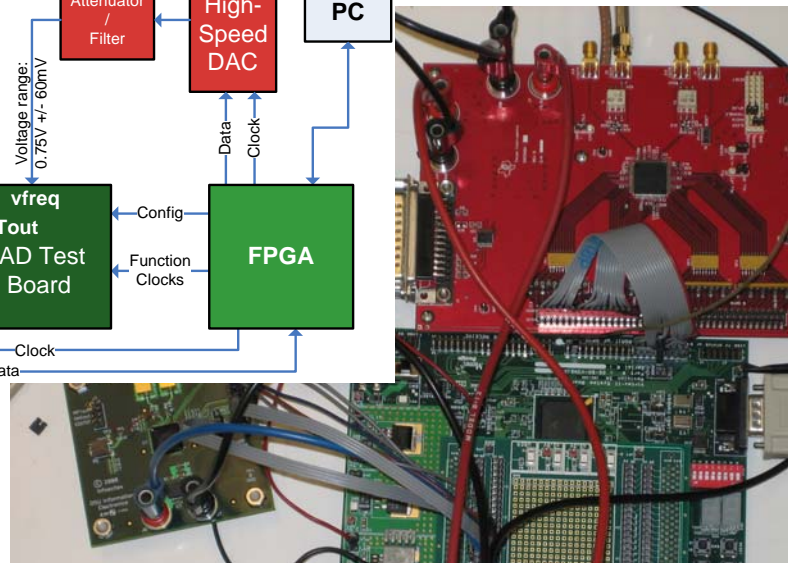
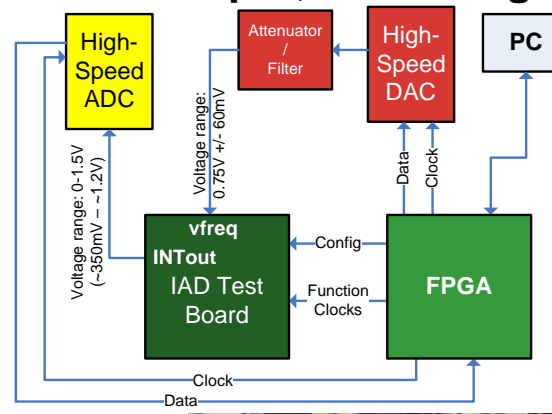
Magnitude and Phase preserved.



Left: 40mV p-p 10MHz input; 250mV p-p step integrated output; 10ns integration time
 Right: 40mV p-p 10MHz input; 50ohm load output; 20ns integration time

FPGA-Based Test Platform

- 500MSPS DAC
- Virtex-II FPGA
 - Config/Control IAD, DAC
 - PC Interface
- ADC interface inwork....



- **Novel aspects of this project:**
 - Basis function approach to sampling theory
 - Reduces the analog baseband requirements
 - Accounts for jitter, synchronization, aperture and matching effects in the sampling theoretic framework
- **Risks/challenges:**
 - Mixed-signal wide-bandwidth integrators
 - Presently requires custom ASIC development
- **Potential applications & benefits:**
 - CMOS implementation for wide bandwidth systems
 - Novel approach to parallel sampling

- **FPGA Test Platform Development**
 - ASIC IAD functions correctly.
 - Integrated DAC and FPGA
 - Matlab constructed OFDM waveform implemented by DAC hardware
 - Created Testboard for packaged IAD device.
 - Integrated FPGA and IAD testboard
 - Created PC Interface
- **Sampling Research**
 - Effects of aperture jitter reduced by Wide Aperture Sampling
 - Effects of clock jitter reduced by Integrated Sampling

- **FPGA Test Platform Development**
 - Complete ADC integration
 - Examine IAD performance on OFDM waveform produced by DAC
 - Create portable IAD demonstration platform
- **Second IAD Tapeout**
 - Add digital mixer to IAD block
 - Increase performance of IAD components
- **Sampling Research**
 - Develop Basis function transformations in FPGAs
 - Continue evaluation of jitter and aperture effect reduction by Integrated Sampling