Research Highlights

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Background

- **Appointments**
  - Feb 15, 2009: Assistant Prof., Electrical Engineering, Ohio State University.
    - Associate Director of Industrial Relations, ElectroScience Laboratory
  - April 1993-Present: Intel Corporation

- **Education**
  - B.S.E.E. w/Honor, University of Minnesota
  - M.S.E.E., University of Minnesota
  - Ph.D., Arizona State University

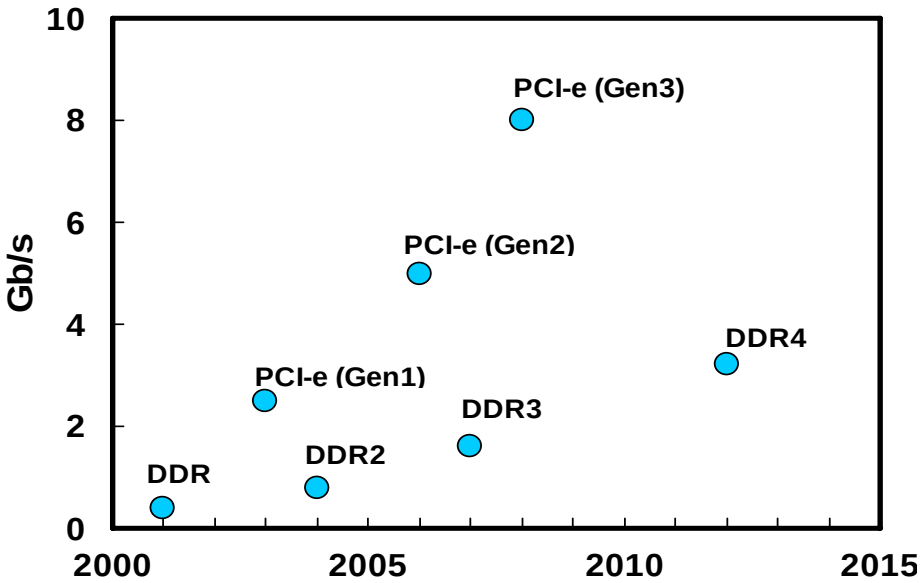
Research Highlights

- Novel Interconnect Technologies
  - Mm-wave Chip-to-Chip interconnect for future technology nodes
    - *Low-cost polymer channels overlay on top of standard FR4 substrate*
    - *Mm-wave I/O circuits on standard CMOS*
- Active Integrated Antennas (AIA)
  - Low-power broadband phase array systems
    - *Power combining in free space eliminates PAs and power combining circuits*
    - *Coupled oscillators design eliminates expensive phase shifters*

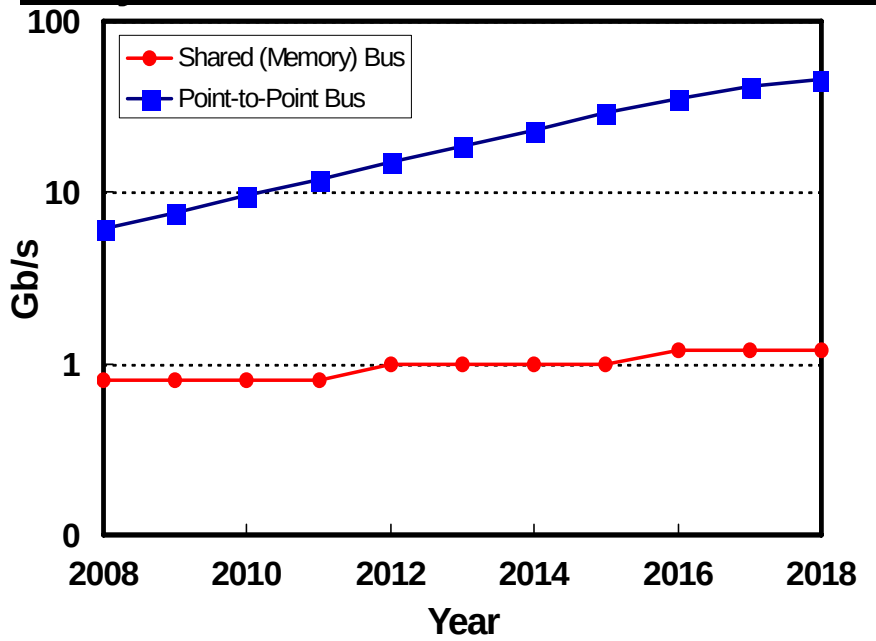
Scalable mm-wave Chip-to-Chip Interconnect on Standard FR4 Boards

The Interconnect Bottleneck

The Picture Today



Projected Demand, ITRS 2007)

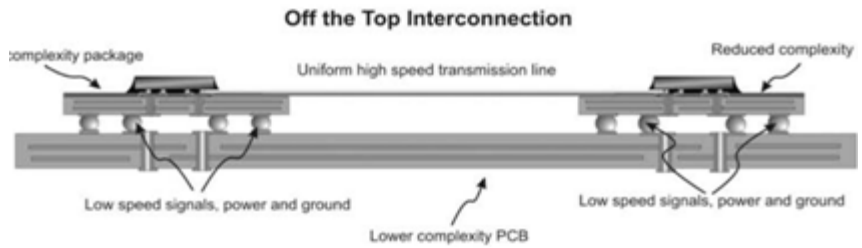


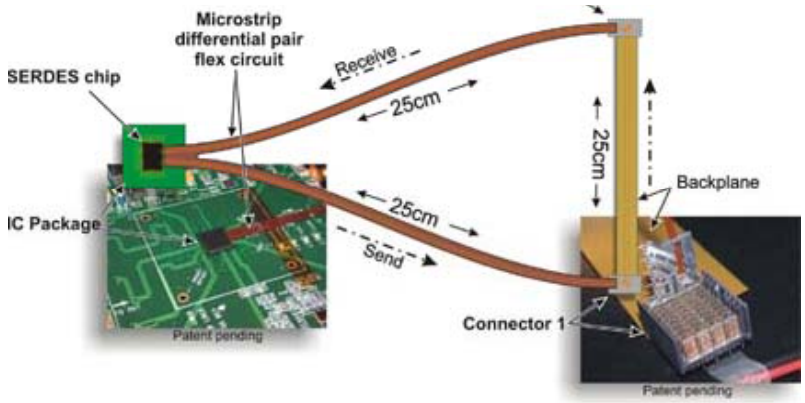
- FR4 dielectric loss at >10 GHz becomes dominant
- Excessive I/O power consumption and thus thermal management are becoming major system issues:
  - Rapid increase in I/O pins to meet BW demand
  - Increased circuit complexity (e.g. equalization, multiple gain stages) to compensate for low signal swing (PCB loss) and distortion (ISI) problems.

Relevant Work

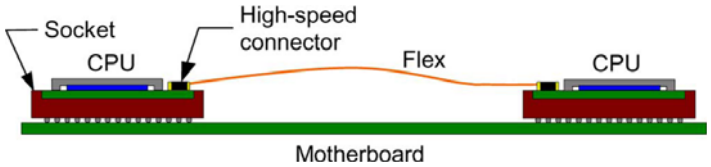
- Optical interconnect can be used ***but*** can not justify cost
- Industry needs a low-cost alternative utilizing exiting motherboard infrastructure

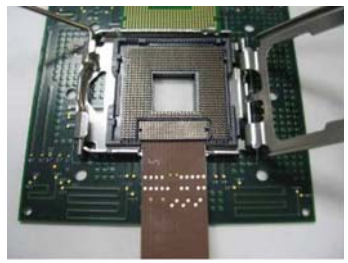
Off the Top Interconnect[1]





Flex-ribbon Interconnect[2]





Flex cable interconnect

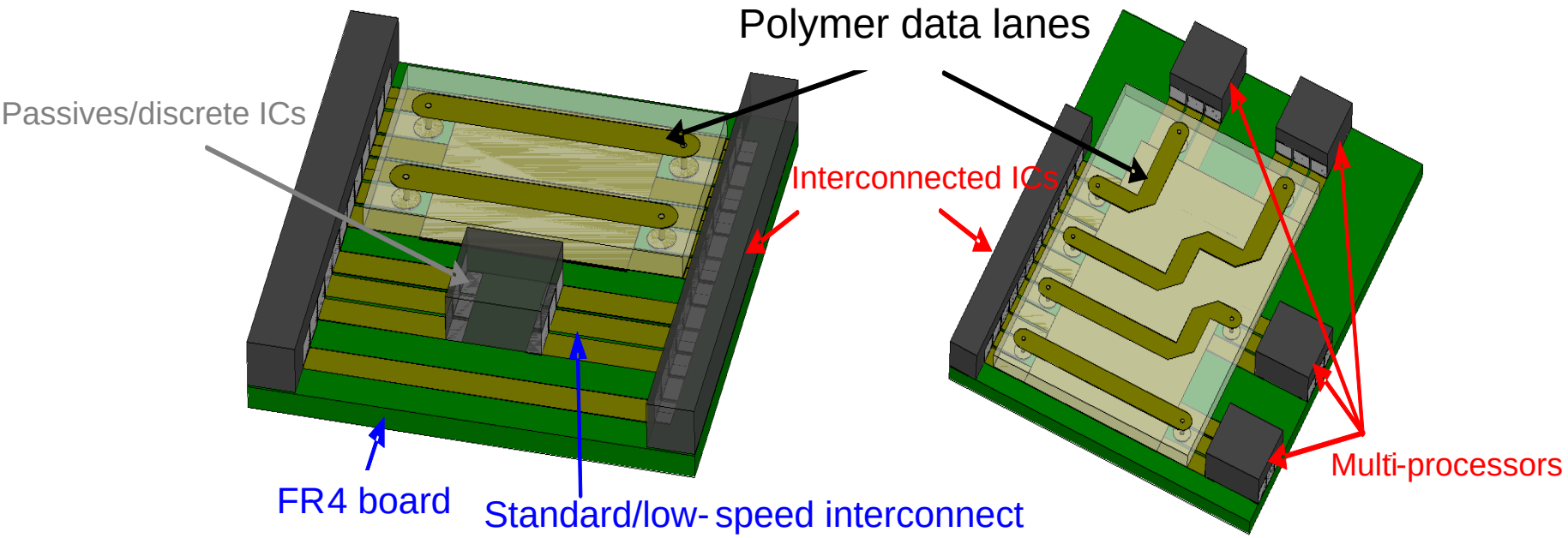
- low-loss dielectric
- Added cost of connector on package-top and/or custom socket

[1] K. Grundy, Proc. DesignCon, 2006

[2] H. Braunisch, *IEEE Trans. on Advanced Packaging*, 2009

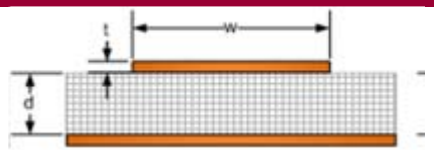
Proposed Technology

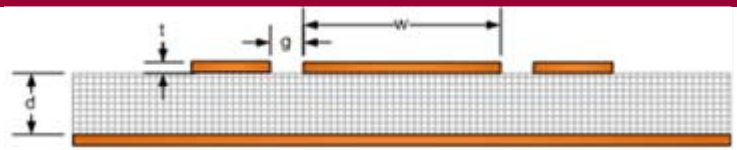
- High speed data lanes overlaid on standard FR4 sub.

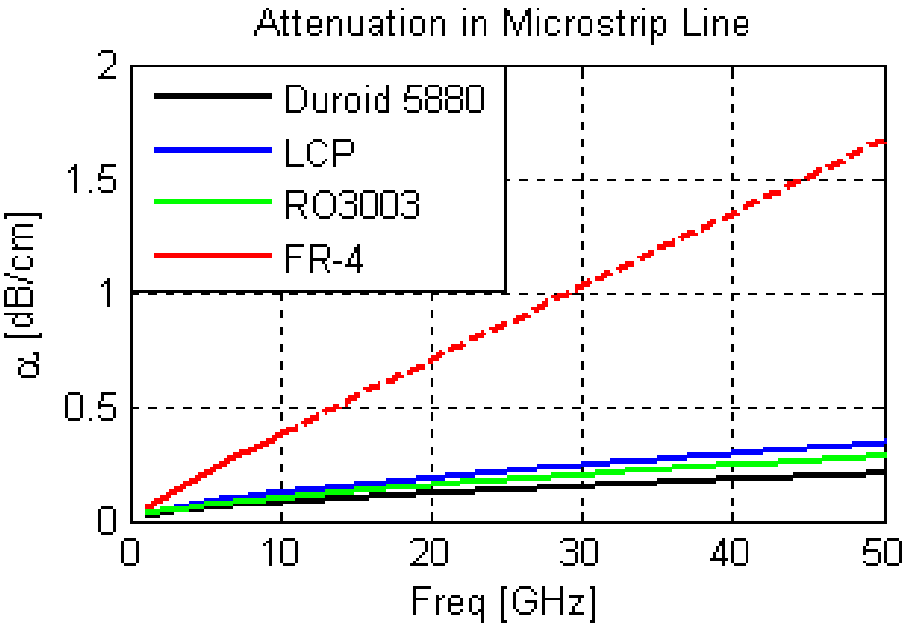


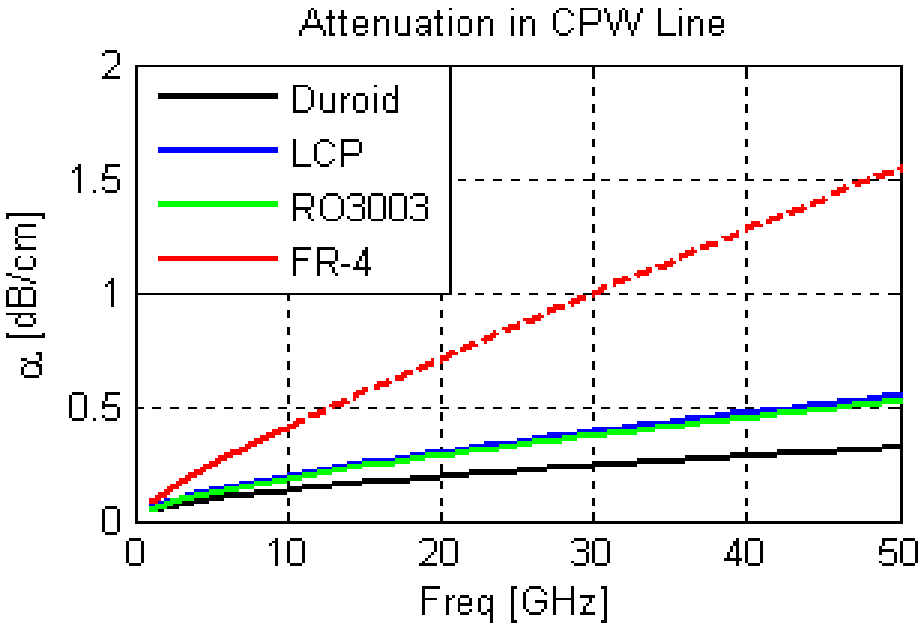
  - Polymer is only used for high speed data lanes and only covers a small portion of the FR4 substrate
  - Polymer deposit is an additive process,
    - Tooling requirements are minimal → small incremental cost
  - Proposed polymer material can withstand high processing and operating temperatures

The Polymer Advantage



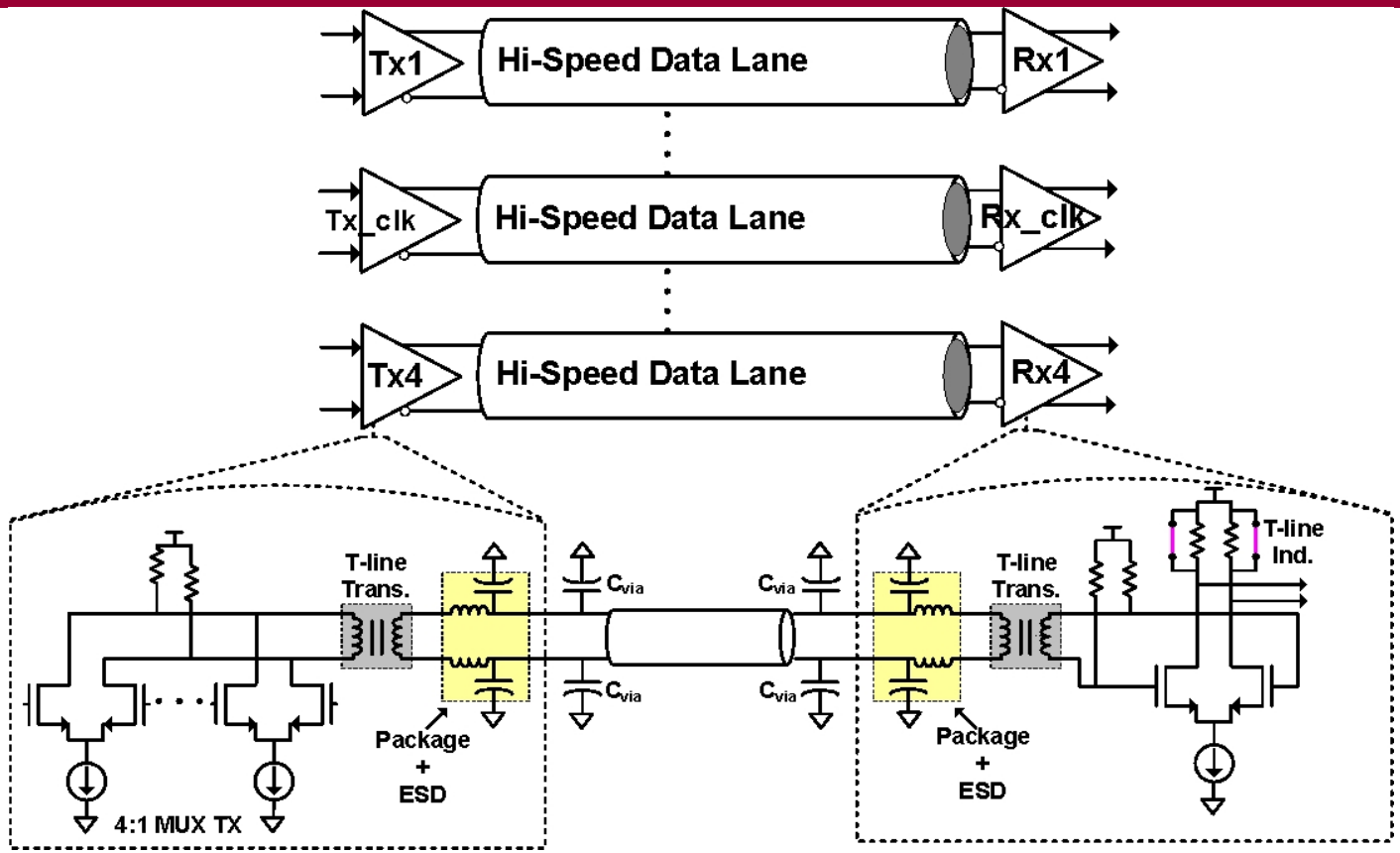






- PTFE, LCP, and BCB offer high melting point (e.g. > 250 °C) and low dielectric loss at mm-wave frequencies
  - Polymer substrate cost is 3-10x FR4 board
- Previous research focused on replacing FR4 w/ polymer substrates
  - Cost prohibitive
- Proposed research targets overlays of small polymer sheets (< 1mm thick) **only** for high speed lanes

CMOS Test Vehicle



- Large cap. loading at TX/RX → significant degradation in return loss at mm-wave frequencies
  - Present art relies on DC-only termination
  - Polymers interconnects address loss problem but ISI becomes dominant
- Utilize T-line transformers to detune cap. and achieve high signal swing at lower current

Risks and Benefits

- **Novel aspects of this project:**
  - Combining low loss properties of polymers and cost advantage of FR4 materials
    - Achieve interconnect speeds up to 50 Gb/s using existing echo system with standard FR4 PCBs
- **Risks/challenges:**
  - Polymer overlay process is not proven technology
    - CTE mismatch between polymer and FR4 substrate
  - CMOS I/O design at mm-wave
    - Building active and passive circuit elements
    - Accurate model of both on-chip and off-chip (i.e. package and board) interconnects and discontinuities
- **Potential applications & benefits:**
  - PC H/W (Intel, IBM, TI, Dell, Micron, etc.), Avionics/Defense (Honeywell, Boeing, NG, etc…), and Telecommunications Equipment (Cisco, etc..) industries